

Duration: 2:30Hrs

Total Marks: 60

**N.B: (1) All questions are compulsory.**

**(2) Figures to the right indicate maximum marks.**

**(3) Use of non-programmable calculators is permitted.**

**(4) Symbols used have their usual meaning**

- Q1. A) Attempt any ONE. (08)**
- 1 Define the Architecture of the VHDL. Explain any one of the Architecture with suitable examples.
  - 2 Explain the Transport versus Inertial Delay in VHDL.
- B) Attempt any ONE. (04)**
- 1 Explain the different terms in VHDL.
  - 2 Write a short note on Entity with a suitable example VHDL.
- Q2. A) Attempt any ONE. (08)**
- 1 Describe briefly about the Signal Object types with a suitable example in VHDL.
  - 2 List the Different Data types. Explain the composite types with an example in VHDL.
- B) Attempt any ONE. (04)**
- 1 Give an Example of Procedures in subprograms of VHDL.
  - 2 Write an example of subprogram Declaration in VHDL.
- Q3. A) Attempt any ONE. (08)**
- 1 Explain the process of Host learnt about the device in USB.
  - 2 Describe briefly about the Control transfer in USB.
- B) Attempt any ONE. (04)**
- 1 Explain USB 2.0 transaction.
  - 2 Write a short note on the topology with diagram using USB 3.0.

- Q4. A) **Attempt any ONE.** (08)
- 1 Explain the 10 bit addressing in I2C bus interfacing
  - 2 Write down about the RS-232, RS-485 and ZigBee in external Communication Interface.
- B) **Attempt any ONE.** (04)
- 1 Explain the IEEE 1394(fire wire) in external communication interface.
  - 2 Describe shortly about the 'transferring data' in I2C bus specification.
- Q5. **Attempt any FOUR.** (12)
- 1 Give an example of wait Time-out VHDL.
  - 2 Define process statement in VHDL.
  - 3 Write an example of Value type attributes VHDL.
  - 4 Write an example of Package body VHDL.
  - 5 Write down about Uses and limits in USB transfer.
  - 6 Draw the diagram of USB 3.0 hosts and hubs supports all four speeds for downstream communications
  - 7 Explain shortly about the 'Start and Stop conditions' in I2C bus interfacing.
  - 8 Write a short note on the 'I2C bus concept'.

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